Almost All-Digital Sinewave-Product Generation for Frequency Synthesis Applications

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***Abstract*— We propose a frequency mixer built from almost exclusively digital components. The circuit produces a sinusoidal signal at frequency $\omega_1 \pm \omega_2$ when its input frequencies are $N\omega_1$ and $N\omega_2$, both provided in the form of digital clocks. As it uses almost exclusively digital circuitry, it can easily be integrated with digital CMOS and possesses many advantages inherent in digital circuits. Predictions of the system's performance have been supported with spectral measurements of a discrete implementation.**

I. Introduction

Frequency mixers are an important component of multiloop frequency synthesizers, which are used in many applications including communications, radar, and instrumentation [1].

The popular frequency mixer is an analog circuit, usually of one of two general forms. The first is the standard diode-based mixer that essentially operates as an analog switch for the RF signal - a pure sinusoid - controlled by the LO signal that is ideally a square-wave [2]. Double-balanced diode mixers is probably the most common representative of this form. The second form is based on the Gilbert cell [3]. If appropriate pre-distortion circuitry is used, the Gilbert cell can operate as a four quadrant linear multiplier as well.

These circuits suffer from the typical drawbacks of analog circuits, such as reduced integrability with digital circuits, higher power consumption/requirement, and lack of technology portability in designs. Additionally, they require that at least one of the input signals is a pure sinusoidal in order to minimize the output spurious frequency components. This typically imposes filtering requirements and constraints in the operating frequency.

The proposed method, being a nearly digital approach, has many of the advantages of digital circuits and additionally does not have the input spectral purity requirements of the analog mixers since it is driven by digital signals. The digital part of the mixer consists of 2 finite state machines (FSM) and a look-up-table (LUT) that generates a digitally coded representation of the output sinusoid. A small nonlinear DAC [4] converts the LUT's digital output into analog form.

II. A Sinusoidal Approximation

We consider approximations of the ideal sinusoid of the following form:

$$a(t) = p_i \ , \quad t \in \left[\frac{iT_1}{N}, \frac{(i+1)T_1}{N} \right), \tag{1}$$

with

$$p_i = \cos\left(\frac{2\pi i}{N} + \theta\right), \tag{2}$$

$\theta \in [0, 2\pi/N)$ and $i = 0, 1, 2, \ldots$. Thus $a(t)$ is a sampled-and-held version of the ideal sinusoid and has period T_1. Fig. 1 shows an example for the case $N = 8$.

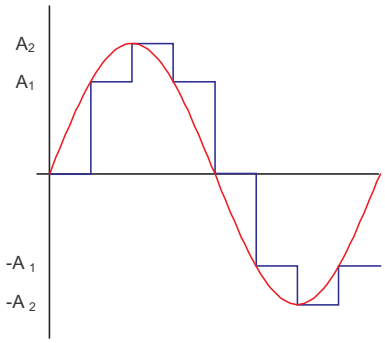

Fig. 1. A sampled and held version of the ideal sinusoid

Note that if N is even, then

$$p_i = -p_{i+N/2} \tag{3}$$

This property will be used in the discussion of the nonlinear DAC later in the paper.

We define a signal $b(t)$ identically as $a(t)$, except with T_2 replacing T_1. It can be shown that signals $a(t)$ and $b(t)$ have harmonics only of the orders $k = (rN+1)$ and $k = (rN-1)$, where $r = 1, 2, 3, \ldots$, i.e., if A_k and B_k are the k^{th} Fourier series coefficients of $a(t)$ or $b(t)$ then

$$A_k = B_k = 0 \text{ for all } k \neq (rN+1), (rN-1).$$

III. Digital Components of the Mixer

This section presents the concepts and circuit implementation of the digital part of the proposed frequency mixer architecture.

A. Digital Representation of signals $a(t)$ and $b(t)$

Consider the approximation signal $a(t)$ in Figure 1. Because it has at most N distinct values, it requires at most $\lceil \log_2(N) \rceil$ bits to represent the corresponding analog form without loss of information. Thus, the digital form of $a(t)$ can be generated with a small finite state machine (FSM). This is depicted in Figure 2, where the sequence d_i is the digital output of the

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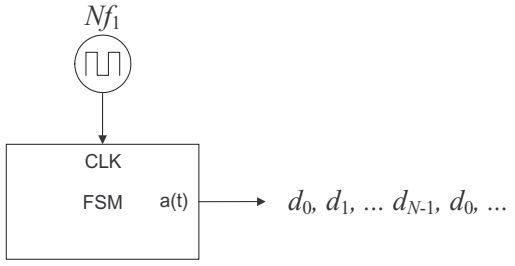

Fig. 2. Representing $a(t)$ with a small FSM

FSM (and has a period of N) and the digital representation of the signal $a(t)$.

The output of the FSM, when viewed as a discrete sequence, has period N, and is at most $\lceil \log_2(N) \rceil$ bits wide. When the input clock to the FSM has fundamental frequency $N\omega_1$, the output will have fundamental frequency ω_1. The signal $b(t)$ is generated similarly with another FSM with clock input of $N\omega_2$.

B. Digital Representation of the product $a(t)b(t)$

Since the digital representations of $a(t)$ and $b(t)$ possess all the necessary information to determine the corresponding analog values, by examining these digital codes, we have all the information necessary to determine the value of the product $a(t)b(t)$. Thus, the product can be computed with a small look-up-table (LUT). This digital code will then be converted into analog form with a nonlinear DAC. The circuit is shown in Fig. 3.

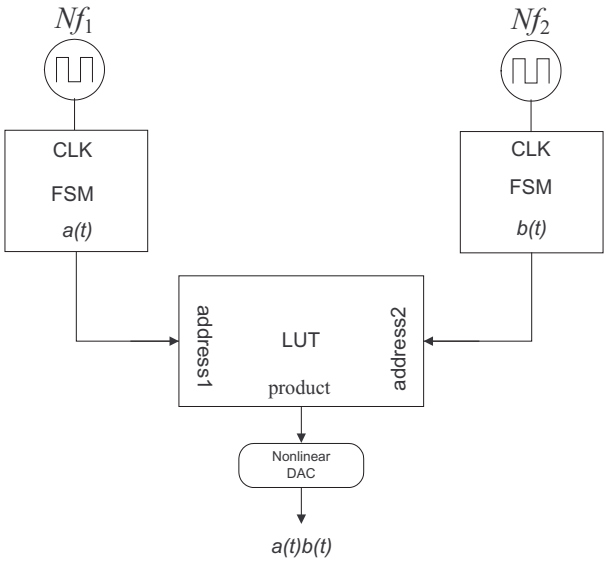

Fig. 3. Generating the digital representation of product $a(t)b(t)$

IV. Nonlinear Digital-to-Analog Conversion

The proposed frequency mixer utilizes a nonlinear DAC. The reason for not using a linear DAC is that the system only needs to produce a small number of possible output (analog) values. These possible values are the products $p_i p_j$, where p_i, p_j are possible values of $a(t)$ (and $b(t)$). Thus, we can construct a DAC that can more efficiently produce only the desired values.

For illustration we will discuss the operation of the proposed nonlinear DAC with 6 resistors, as shown in Figure 4. The input to the DAC is a 6-bit digital signal $(V_2, V_1, V_0, W_2, W_1, W_0)$ and the output of the DAC is V_{out}. We can consider the digital signal $(V_2, V_1, V_0, W_2, W_1, W_0)$ as an analog signal taking values 0 and 1 V. Then the output of the DAC can be expressed as

$$V_{out} = c\left(\frac{V_2}{R_2} + \frac{V_1}{R_1} + \frac{V_0}{R_0} + \frac{W_2}{R_2} + \frac{W_1}{R_1} + \frac{W_0}{R_0}\right),$$

where

$$c = \frac{1}{\frac{2}{R_0} + \frac{2}{R_1} + \frac{2}{R_2}}$$

is a constant that depends on the choice of the resistors.

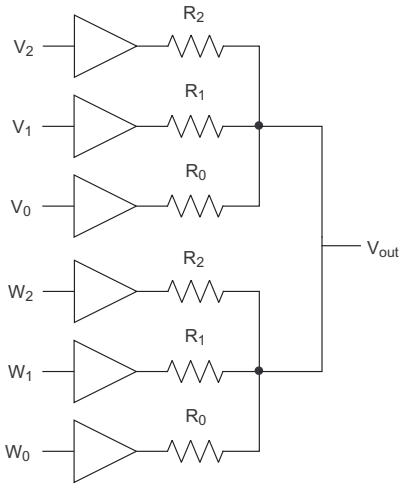

Fig. 4. Nonlinear DAC, for the case $2B = 6$

Since the output of the DAC is always non-negative, we generate the output sinusoidal (AC) with a certain positive DC offset.

Using a general DAC with $2B$ resistors, we can produce an output of the form

$$c\sum_{i=0}^{B-1}\frac{s_i}{R_i} + c\sum_{i=0}^{B-1}\frac{1}{R_i} \tag{4}$$

where $s_i \in \{-1, 0, 1\}$ and

$$c = \frac{1}{\sum_{i=0}^{B-1}\frac{2}{R_i}}$$

First consider the generation of an AC output of 0. This is achieved with an input of $V = 00\cdots0$ and $W = 11\cdots1$. This produces an analog output of

$$K = c\sum_{i=0}^{B-1}\frac{1}{R_i} \tag{5}$$

Let this be defined as output which corresponds to an AC value of 0; in other words, this is the DC offset at the output. This corresponds to having all $s_i = 0$ in (4).

When can rewrite the DAC output as

$$V_{out} = c \sum_{i=0}^{B-1} \frac{s_i}{R_i} + K$$

Let us first make the inputs be $V = 00\cdots0$ and $W = 11\cdots1$, resulting in $s_i = 0$ for all i. Now make the change $V_j = 1$. The resulting output is thus increased by c/R_j, yielding

$$V_{out} = c/R_j + K$$

This corresponds to making $s_j = 1$ and keeping all other $s_i = 0$.

Let us restore $V_j = 0$ as before. Suppose we instead change W_j to 0. Then the output is now c/R_j smaller than before:

$$V_{out} = -c/R_j + K$$

Thus, we have made $s_j = -1$ and kept all other $s_i = 0$.

These operations can be done independently for any V_j and W_j to choose any $s_j \in \{-1, 0, 1\}$, thus arriving at (4).

The mixer must generate the products (analog values) $p_i p_j, i, j = 0, 1, \ldots, N-1$, where p_i are the analog values of $a(t)$ and $b(t)$. If N is not large, then the number of products that need to be synthesized will be reasonably small and can be accurately generated with the nonlinear DAC. The complete system is depicted in Figure 5.

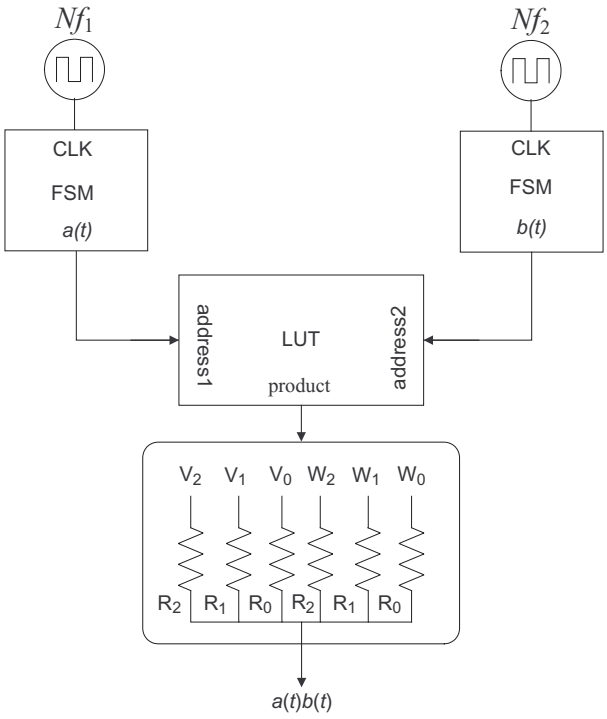

Fig. 5. Complete single-phase mixed-signal mixer

As mentioned earlier, if N is even then $a(t)$ (and $b(t)$) takes values that occur in oppositely-signed pairs (i.e., if one possible value is p_0, then $-p_0$ will also be one of the values). Thus, the values of $a(t)b(t)$ occur in oppositely-signed pairs as well. It can be shown that a product signal $a(t)b(t)$ of this form will lack all intermodulation products of the form

$$k\omega_1 \pm m\omega_2, \ k \text{ or } m \text{ even}$$

regardless of the choice of the resistors R_i. Thus, such intermodulation products will be absent even if the DAC's output is a poor approximation of the product $a(t)b(t)$.

V. Simulation and Measurement

The digital components of the proposed frequency mixer were built using an FPGA. The nonlinear DAC consisted of $2B = 8$ discrete resistors. We chose $a(t)$ and $b(t)$ to have $N = 10$ partitions of their periods.

To obtain the parameter θ of (2) and the values of the resistors, we employed numerical optimization under a set of constraints which would be reasonably to impose in a monolithic implementation. We constrained all resistor values to be integer multiples of 50 ohms and that their sizes be limited. Chosing the objective of minimum mean square error in approximating the product $a(t)b(t)$, our optimization algorithm arrived at a solution of $\theta = 0.314159$ rad and the resistances in table I.

resistor	multiple of reference (50 Ohm)	resistance
R_0	6	300
R_1	7	350
R_2	12	600
R_3	23	1150

TABLE I

Resistor values for test circuit

Table II lists all the possible non-negative products (in a normalized form) corresponding to our choice of $a(t)$. From table II, one can see that the ideal values of the product $a(t)b(t)$ are closely approximated by the output of the chosen nonlinear DAC. Because of the symmetry of the DAC, the negative outputs are exactly the negative of the positive ones (assuming matched resistors).

exact product (normalized)	resistor network approximation of product (normalized)
0	0
0.1714118	0.1714133
0.2773501	0.2773489
0.4487619	0.4487623

TABLE II

All possible non-negative products for test circuit

Fig. 6 shows a MATLAB simulation of the output spectrum for input frequencies of $Nf_1 = 6.73$ MHz and $Nf_2 = 10$ MHz and resulting output difference frequency $f_{out} = 327$ kHz. Fig. 7 shows the corresponding measurement.

Fig. 8 shows the output waveform of the DAC when one of the inputs to the mixer is constant (frequency of 0) and the other is 10 MHz (resulting in output of 1 MHz).

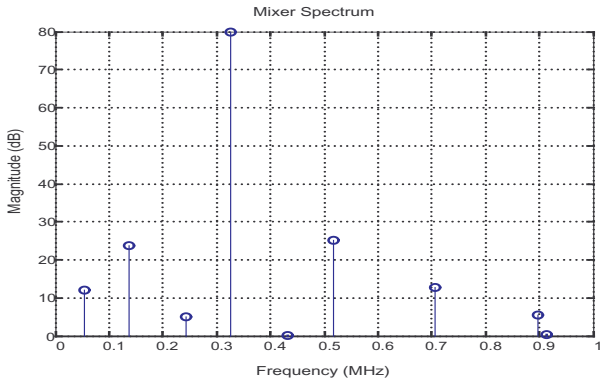

Fig. 6. Simulated spectrum of a single phase mixer for input frequencies $Nf_1 = 6.73$ MHz and $Nf_2 = 10$ MHz

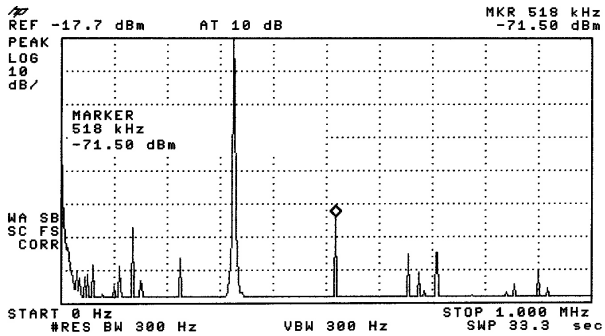

Fig. 7. Spectrum of a single phase mixer for input frequencies $Nf_1 = 6.73$ MHz and $Nf_2 = 10$ MHz

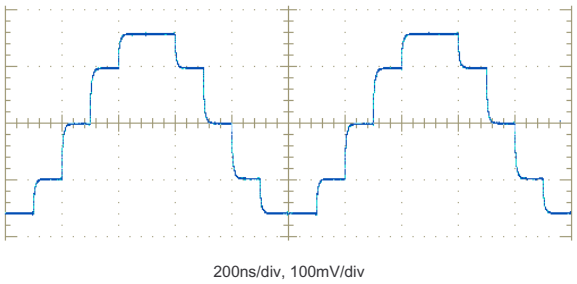

Fig. 8. Output of frequency mixer with one input being 10 MHz and the other being constant.

VI. Conclusions

We have presented a nearly fully digital frequency mixer offering the advantages found in digital circuits as well as the convenience of using digital input signals.

An discrete test circuit demonstrated the feasibility of the proposed method.

Despite errors introduced primarily by the non-ideal output impedances of the output digital drivers, measurements matched simulations sufficiently well.

We expect greatly improved performance in a monolithic implementation due to reduced mismatch errors, elimination of most PCB-level parasitics and layout circuit optimization. A current-mode nonlinear DAC would also provide significant improvement.

References

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